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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,335	07/24/2003	Vincent J. Jorgensen	X-1251 US	2274

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EXAMINER	
KIM, EUNHEE	

ART UNIT	PAPER NUMBER
2123	

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05/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,335	JORGENSEN, VINCENT	
	Examiner	Art Unit	
	Eunhee Kim	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/13/2007 has been entered.

2. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-14 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joly et al. (US Patent No. 6,345,378), in view of Kuribayashi et al. (US Patent Number 6,374,205), in view of Wirthlin et al. (US Patent No. 6,173,434), and further in view of Bryant et al. (US Patent No. 6,968,487)

Regarding Claims 1, 11, 16, and 18,

Joly et al. teaches a method and system of reducing a size of a netlist for a target architecture (Abstract) for simulation and machine readable storage (Fig. 1), having stored thereon a computer program having a plurality of code sections executable by a machine (Fig. 1), comprising:

(Claims 1, 11, 16, and 18) create a netlist of objects for the target hardware architecture (Fig. 2, Col. 6 lines 1-51);

(Claims 1, 16, and 18) identify objects specific to the target hardware architecture that are repeated to identify potential dummy objects (Fig. 3-8, Col. 4 lines 46-67, Col. 6 lines 33-50, Col. 8 lines 50-54, Col. 9 lines 31-67, Col. 10 lines 1-33);

(Claim 11) emptying the repeated objects found on the list of repeated objects forming a plurality of dummy objects netlist (Fig. 2-9, Fig. 14, Appendices A-C, Col. 4 lines 46-67, Col. 11 lines 25-67, Col. 13 lines 53-65, Col. 14 lines 16-50);

(Claims 1, 16, and 18) create a list of objects, from the netlist of object, that are used by a circuit design to be implemented in the target hardware architecture (Fig. 3-8, Col. 4 lines 46-67, Col. 6 lines 25-67, Col. 7 lines 1-16, Col. 12 lines 1-67, Col. 13 lines 1-52);

(Claims 1, 16, and 18) the list of objects used by the circuit design (Fig. 2-7, Col. 6 lines 1-67, Col. 7 lines 1-16, Col. 12 lines 3-16).

Joly et al. does not teach (Claims 1, 16, and 18) the step of simulating the modified netlist;

(Claims 1, 16, and 18) form a list of unused objects in the target hardware architecture from the netlist of objects;

(Claims 1, 11, 16, and 18) replace at least one object in the netlist of objects for the target hardware architecture that is also specified in the list of unused objects with an appropriate dummy object to form a modified netlist;

(Claim 11) parsing a programmatic circuit description to be implemented in the target hardware architecture to extract a list containing object names for all used objects for the target architecture;

(Claim 11) parsing a netlist of objects line by line for the target architecture;

Kuribayashi et al. teach (Claims 1, 16, and 18) the step of simulating the modified netlist (Abstract, Fig. 1, Col. lines 49-61);

(Claim 11) parsing a file to extract a list containing object names for all used objects for the target hardware architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49-67); and

(Claim 11) parsing a netlist of objects line by line for the target architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49-67).

Wirthlin et al. teaches (Claims 1, 16, and 18) form a list of unused objects in the target hardware architecture from the netlist of objects (Fig. 3, Col. 5 lines 27-63).

Bryant et al. teaches (Claims 1, 11, 16, and 18) replace at least one object in the netlist of objects for the target hardware architecture that is also specified in the list of unused objects with an appropriate dummy object to form a modified netlist (Col. 6 lines 26-30).

Joly et al., Kuribayashi et al., Wirthlin et al., and Bryant et al. are analogous art because they are both related to a method of reducing circuit data.

Therefore, it would have been obvious to one of ordinary skill in the art of at the time the invention was made to include the teachings of Kuribayashi et al., a list of unused objects of Wirthline et al., and dummy replacement of Bryant et al., in the method for synthesis shell generation with dummy shell of Joly et al. because simulating the modified netlist, parsing a file to extract a list containing object names for all used objects for the target architecture, and parsing the netlist for the target architecture are well known process in a method of reducing a netlist of circuit. Kuribayashi et al. teach an improved circuit simulating system that provides an accurate reduction and a shortening a simulation time while maintaining the accuracy of

simulation (Col. 3 lines 30-59), and Wirthlin et al. teach an improved system that provides efficient relocating logic array modules (Abstract, col. 3 lines 39-40, Summary of the Invention). Further, dummy replacement is a well known process in a method of reducing a netlist of circuit, and Bryant et al. teaches advantages system that can be easily adapted for use in both integrated circuits requiring large FPGAs and ICs requiring small FPGAs (Col. 4 lines 5-15).

Regarding Claim 2,

Joly et al. teach the steps of subtracting the list of objects used by the circuit design from the netlist of objects (Fig. 2-7, Col. 6 lines 1-67, Col. 7 lines 1-16).

Regarding Claim 3,

Joly et al. teach the step of replacing objects in the netlist of objects for the target hardware architecture that is also specified in the list of unused objects that are repeated with the appropriate dummy objects to form the modified netlist (Fig. 2-9, Appendices A-C, Col. 4 lines 46-67, Col. 6 lines 33-67, Col. 11 lines 25-67, Col. 4 lines 46-67, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claim 4,

Joly et al. teach the step of replacing each object in the netlist of objects for the target hardware architecture that is also specified in the list of unused objects with the object with the appropriate dummy object to form the modified netlist (Fig. 2-9, Appendices A-C, Col. 4 lines

46-67, Col. 6 lines 33-67, Col. 11 lines 25-67, Col. 4 lines 46-67, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claims 5, 7, 17, and 19,

Joly et al. teaches (Claim 7, 17, and 19) forming a modified netlist with the appropriate dummy objects when all lines of the netlist have been parsed (Appendices A-C, Fig. 3-8, Col. 8 lines 50-54, Col. 9 lines 31-67, Col. 10 lines 1-33, Col. 11 lines 25-67, Col. 14 lines 16-50).

Joly et al. fail to teach (Claims 5, 7, 17, and 19) the steps of parsing a file to extract a list containing object names for all used objects for the target hardware architecture and parsing the netlist for the target hardware architecture line by line.

Kuribayashi et al. teach the steps of parsing a file to extract a list containing object names for all used instances for the target hardware architecture and parsing the netlist for the target hardware architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49-67).

Regarding Claim 6,

Joly et al. teach the step of replacing a type of an instance for an object found in the repeated list of objects with a type for a corresponding dummy object if the object found in the repeated list is not on the list containing object names for all used objcets (Fig. 2-9, Appendices A-C, Col. 4 lines 46-67, Col. 6 lines 33-67, Col. 11 lines 25-67, Col. 4 lines 46-67, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claims 8 and 12,

Joly et al. teach the step of feeding through a signal unchanged when simulating the appropriate dummy object during a simulation process using the modified netlist (Appendices A-C, Fig. 3-8, Fig. 14, Col. 8 lines 50-54, Col. 9 lines 31-67, Col. 10 lines 1-33, Col. 11 lines 25-67, Col. 14 lines 16-50).

Regarding Claim 9,

Joly et al. teach the step of manually composing a list of repeated listed of root objects specific to the target hardware architecture (Fig. 2, Col. 5 lines 57-65, Col. 8 lines 55-64, Col. 12 lines 17-44).

Regarding Claims 10, 13, and 20,

Joly et al. teach the step of using a Verilog version (Col. 5 lines 57-67, Col. 14 lines 17-19) and emptying a hardware description language version of a repeated object to form an object devoid of an explicit functional mapping of an input to an output (Fig. 2-9, Appendices A-C, Col. 4 lines 46-67, Col. 5 lines 57-67, Col. 6 lines 33-67, Col. 11 lines 25-67, Col. 4 lines 46-67, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claim 14,

Joly et al. teaches the step of parsing a file containing hierarchical path names (Appendices A-C, Fig. 4, Col. 7 lines 38-64, Col. 7 lines 2-49, Col. lines 17-50).

Joly et al. fails to teach the memory blocks of a field programmable gate array forming the target hardware architecture.

Wirthlin et al. teach the steps the memory blocks of a field programmable gate array (Abstract, Fig. 2A-2F and 3).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joly et al. (US Patent No. 6,345,378), in view of Kuribayashi et al. (US Patent Number 6,374,205), in view of Wirthlin et al. (US Patent No. 6,173,434), and in view of Bryant et al. (US Patent No. 6,968,487), and further in the view of Rupp et al. (US Patent Number 6,857,110).

Joly et al. as modified by Kuribayashi et al. Wirthlin et al., and Bryant et al. teach most all of the instant invention as applied to claims 1-14 and 16-20 above.

Joly et al. as modified by Kuribayashi et al. Wirthlin et al., and Bryant et al. teach the step of generating a file containing hierarchical path names (Joly et al.: Appendices A-C, Fig. 4, Col. 7 lines 38-64, Col. 7 lines 2-49, Col. lines 17-50 and Kuribayashi et al.: Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49-67).

Joly et al. as modified by Kuribayashi et al. Wirthlin et al., and Bryant et al. fail to teach the converting bitstream names into Verilog hierarchical path names.

Rupp et al. teach the converting bitstream names into Verilog hierarchical path names (Fig 13-16, Col. 16 lines 22-67, Col. 17 lines 1-15).

Joly et al. as modified by Kuribayashi et al. Wirthlin et al., and Bryant et al. and Rupp et al. are analogous art because they are both related to a method of simulating circuit data.

Therefore, it would have been obvious to one of ordinary skill in the art of at the time the invention was made to include the teaching of Rupp et al. of, in the method for simulating the reduced net list generation with dummy shell of Joly et al. as modified by Kuribayashi et al. because the converting bitstream names into Verilog hierarchical path names is well known process in a method of simulating a circuit data. Rupp et al. teach an improved system that incorporates a programmable logic core design and provides signal interface between programmable gate array such as MSA (Abstract, Col. 1 lines 35-55).

Response to Arguments

8. Applicant's arguments filed 04/13/2007 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 1, 11, 16, and 18 have been considered but are moot in view of the new ground(s) of rejection.

Applicant contents that Joly et al. does not teach the limitations that "identify objects specific to the target architecture that are repeated to identify potential dummy objects". The examiner respectfully disagrees because Joly et al. teaches elements/gates deleted marked with an "X"(Col. 8 lines 50-54, Col. 9 lines 31-33) that are corresponding to "identify objects specific to the target architecture that are repeated to identify potential dummy objects".

Applicant contents that the dummy cells of Joly et al. are synthesized and the dummy objects recited in claims 1, 11, 16, and 18 are unrelated.

The examiner agrees, but the examiner relies upon the teaching in Joly et al. to teach the limitation of dummy cells and Kuribayashi is relied upon for a teaching of "the step of simulating the modified netlist ". And the examiner is relied upon on the combination of teachings. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In addition, in response to applicant's arguments that the dummy objects recited in claims 1, 11, 16, and 18 are unrelated, the examiner respectfully disagrees. Applicant's specification indicates that reducing netlist size using a technique termed as Dummy Block Replacement (DBR) ([0006] of page 3) and DBR can then essentially selectively "remove" unused blocks and the act of "removing", "emptying or "replacing" an object or instance should be understood herein as creating an instance of a module without any functional mapping or that is empty (line 8-13 on page 5). Joly et al. set forth the reduced set forth the reduced netlist that has a dummy cell corresponding to an instance of a module without any functional mapping, represented by the schematic in Fig. 14. Hence, the office takes the position that Joly et al. teach and disclose the limitation cited above in Fig. 2-9, Fig. 14, Appendices A-C, on Col. 4 lines 46-67, on Col. 6 lines 1-67, on Col. 7 lines 1-16, on Col. 8 lines 50-54, on Col. 9 lines 31-67, on Col. 10 lines 1-33, on Col. 11 lines 25-67, on Col. 4 lines 46-67, on Col. 13 lines 53-65, and on Col. 14 lines 16-50.

Applicant contents that Joly et al. does not teach the limitations that "create a list of objects, from the netlist of objects, that are used by a circuit design to be implemented in the target hardware architecture".

The examiner respectfully disagrees because Joly et al. teaches a block loading file containing the loading information for all the components and nets of the original design (Col. 12 lines 3-4), and a block loading file that is corresponding to a list of object "that are used by a circuit design to be implemented in the target hardware architecture".

Applicant contents that Joly et al. does not teach the limitations "form a list of unused objects in the target hardware architecture from the netlist of objects and the list of objects used by the circuit design".

The examiner disagrees that form "a list of objects used by the circuit design" because Joly et al. teaches the original shell netlist files corresponding to a list of objects used by the circuit design (Col. 12 lines 3-16).

However, the examiner agrees that Joly et al. does not teach the limitations "form a list of unused objects in the target hardware architecture from the netlist of objects", thus upon further consideration, a new ground(s) of rejection is made in view of Kuribayashi et al. Wirthlin et al., and Bryant et al..

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Greidinger et al. discloses Method for designing large standard-cell base integrated circuits (US Patent No. 6567967).

Shackleford discloses graph partitioning engine based on programmable gate array (US Patent No. 5761077).

Huang et al. disclose a partitioning-based standard-cell global placement (Partitioning-based standard-cell global placement with an exact objective).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eunhee Kim whose telephone number is 571-272-2164. The examiner can normally be reached on 8:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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